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	Application No.	Applicant(s)	
N. 43	10/708,228	YANG ET AL.	
Notice of Allowability	Examiner	Art Unit	
	William M. Brewster	2823	
The MAILING DATE of this communication appeal All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RI of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in this app or other appropriate communication GHTS. This application is subject to	olication. If not include will be mailed in due of	ed course. THIS
1. This communication is responsive to <u>18 February 2004</u> .			•
2. The allowed claim(s) is/are <u>9-12</u> .			
3. The drawings filed on 18 February 2004 are accepted by the	ne Examiner.		
 4. Acknowledgment is made of a claim for foreign priority una a) All b) Some* c) None of the: Certified copies of the priority documents have Certified copies of the priority documents have Copies of the certified copies of the priority documents have Copies of the certified copies of the priority documents have International Bureau (PCT Rule 17.2(a)). 	been received. been received in Application No. 10		ion from the
* Certified copies not received:			
Applicant has THREE MONTHS FROM THE "MAILING DATE" noted below. Failure to timely comply will result in ABANDONM THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.		complying with the req	uirements
5. A SUBSTITUTE OATH OR DECLARATION must be submit INFORMAL PATENT APPLICATION (PTO-152) which give			OTICE OF
6. CORRECTED DRAWINGS (as "replacement sheets") mus	et be submitted.	•	
(a) ☐ including changes required by the Notice of Draftspers	on's Patent Drawing Review (PTO-	948) attached	
1) hereto or 2) to Paper No./Mail Date			
(b) including changes required by the attached Examiner's Paper No./Mail Date	s Amendment / Comment or in the C	office action of	
Identifying indicia such as the application number (see 37 CFR 1. each sheet. Replacement sheet(s) should be labeled as such in the	.84(c)) should be written on the drawir he header according to 37 CFR 1.121(c	ngs in the front (not the	back) of
7. DEPOSIT OF and/or INFORMATION about the deposit attached Examiner's comment regarding REQUIREMENT I			lote the
Attachment(s) 1. ☑ Notice of References Cited (PTO-892)	5. ☐ Notice of Informal P	atent Application (PTC)-152)
2. Notice of Draftperson's Patent Drawing Review (PTO-948)	6. Interview Summary	(PTO-413),	
3. Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date	Paper No./Mail Dat 8), 7. ⊠ Examiner's Amendn	e nent/Comment	
4. Examiner's Comment Regarding Requirement for Deposit	8. X Examiner's Stateme	ent of Reasons for Allow	wance
of Biological Material	9. Other		

Application/Control Number: 10/708,228

Art Unit: 2823

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

a) In the Title:

After "Memory", insert -- Including a First and Second Exposures to a Photoresist Layer--

Reasons for Allowances

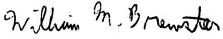
The following is an examiner's statement of reasons for allowance: as opposed to Tanaka, claim 9, lines 10-31, contain the features of, "performing a first exposure process to transfer a pattern in a first photomask to the negative photoresist layer, wherein the pattern in the first photomask corresponds to each memory cell in the memory cell region, and a non-crosslinked portion of the negative photoresist layer is positioned above the channel region of each memory cell in the memory cell region; performing a second exposure process to transfer a pattern in a second photomask to the negative photoresist layer, wherein the pattern of the second photomask precisely corresponds to at least one pre-coding memory cell region in the memory cell region and the gates of the transistors in the periphery circuit region, and non-crosslinked portions of the photoresist layer are positioned above the pre-coding memory cell region

in the memory cell region and above the gates of the transistors in the periphery circuit region, performing a development process to pattern the negative photoresist layer, and performing an ion implantation process to the precoding memory cell region and to adjust a threshold voltage of the transistors using the patterned negative photoresist layer as a mask." The prior art of record fails to teach, in combination, the process features.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 571-272-1854. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



19 August 2005

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